ABSTRACT OF DISCLOSURE

A semiconductor memory device may include an oscillator circuit for generating an oscillation signal that is varied based on mode of operation, and a word line enable circuit for generating a word line enable signal in response to the oscillation signal. The device may also include a control circuit to control the oscillator circuit and the word line enable circuit, so as to control a pulse width of the word line enable signal and period of the oscillation signal, based on a change in operation mode of the device.